## REMARKS/ARGUMENTS

The Applicant has carefully considered this Application in connection with the Examiner's Final Action and respectfully requests reconsideration of the Application in view of the following remarks.

The Applicants originally submitted Claims 1-20 in the application. In this response, the Applicants have resubmitted Claims 1-20 without amendment. Accordingly, Claims 1-20 are currently pending in the application.

### I. Formal Matters and Objections

The Examiner has objected to the Drawings under 37 C.F.R. 1.83(a), which reads in part, "The drawing in a nonprovisional application must show every feature of the invention specified in the claims." Specifically, the Examiner asserts that the element of Claims 5 and 12, "interim results are unavailable to an external program executing in said processor," and Claim 19, "interim results are unavailable to an external program executing in said DSP," are not shown specifically in the drawings. The Applicants respectfully disagree. Figure 4, which illustrates a two-stage MAC 310 constructed according to the principles of the present invention, includes registers 430-435, which provide temporary storage of results from the multiply stage 410 until the accumulate stage 420 becomes available. Specification, ¶¶ 55, 61. All outputs from these registers are provided to the accumulate stage 420, and to nowhere else. In this way, the interim results of the multiply stage 410 are denied to a data bus external to the MAC 310, and there is no communication of the interim results outside the MAC. Thus the elements of Claims 5, 12, and 19 recited above are specifically shown in Figure 4 by the absence of a means to communicate interim results to an external program

executing in the processor. The Applicants therefore respectfully request that the Examiner withdraw the objection to the drawings.

## II. Rejection of Claims 1-20 under 35 U.S.C. §103

In the previous Office Action, the Examiner rejected Claims 1-20 under 35 U.S.C. § 103(a) as being unpatentable over Motorola, Inc. (MPC7410 RISC Microprocessor Technical Summary), in view of Morris (Computer Architecture: The Anatomy of Modern Processors). Specifically, the Examiner asserted that each element of independent Claims 1, 8 and 15 read on the combination of Motorola and Morris, and further, that one of ordinary skill in the art would be motivated to combine Motorola and Morris. The Examiner interpreted the Applicants' arguments in response to be arguing a feature of the invention not specifically stated in the claim language. The Applicant's respectfully disagree.

The Examiner cites the Applicants' arguments from their previous response as follows:

> [T]he Examiner admits that Motorola is silent regarding out-of-order completion logic, but looks to Morris to provide the general background of processor architecture to show that the MPC7410 processor uses pipeline registers. The Examiner continues, referring to the MPC7410 processor in paragraph 22 of the response, "The pipeline registers of the floating-point unit are part of the out-of-order completion logic, associated with said MAC." This assertion is clearly erroneous for the reasons set forth below.
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> The pipeline registers of the MPC7410 processor cannot be properly construed as out-of-order completion logic, as recited in independent Claims 1, 8, and 15. The present invention introduces the broad concept of pipelining a MAC and employing logic to support out-of-order completion to allow the MAC to operate at a higher throughput than was previously possible. As illustrated in one embodiment of the invention, the out-of-order completion is supported by out-of-order completion logic that is physically divided between the instruction issue (ISU) block and the write-back (WB) stage of the pipeline. Specification, ¶ 47. Further, the portion of the out-of-order completion logic located in the ISU may be used to group MAC instructions appropriately. Id., ¶ 48. The grouping rules applied by the ISU are shown in Table 2. These rules are a sophisticated logical algorithm designed to efficiently group

> processor instructions so as to maximize processing speed by maximizing utilization of resources. The grouping algorithm allows instructions to be reordered to achieve the desired resource utilization. Pipeline registers, in contrast, simply store the state of a particular stage in a pipeline for the duration of a single clock period while latencies in the processor settle. Pipeline registers have no ability, inherent or otherwise, to modify the order of operand processing in the processor. Simply put, pipeline registers are not out-of-order completion logic.

Contrary to the Examiner's assertion, the Applicants' arguments do not argue a feature not specifically stated in the claim language. These arguments serve to direct the Examiner to those portions of the Specification that describe embodiments of the invention. Specifically, the features of the invention argued are "pipeline processing multiply-accumulate instructions," line 10 and "out-of-order completion," line 11. These features are claimed in Claim 1, for example, as "pipeline processing multiply-accumulate instructions," and "out-of-order processing," respectively. The arguments recited in lines 12-21 describe an embodiment of the claimed invention, but do not argue a feature not appearing in the claims. Lines 21-24 merely characterize the operation of the pipeline registers in the references cited by the Examiner. Thus, the Examiner's characterization of these arguments as arguing a feature not specifically stated in the claim language is incorrect. Therefore, the Applicants respectfully request that the Examiner withdraw the rejection of Claims 1-20.

## IV. Conclusion

In view of the foregoing amendments and remarks, the Applicants view all of the Claims currently pending in this application to be in condition for allowance and therefore earnestly solicit a Notice of Allowance for Claims 1-20.

The Applicants request the Examiner to telephone the undersigned attorney of record at (972) 480-8800 if such would further or expedite the prosecution of the present application.

Respectfully submitted,

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